IN THE CLAIMS

1-2. (canceled)

3. (previously presented) The integrated signal isolator of claim 37 wherein the input strap includes a plurality of turns.

4. (previously presented) The integrated signal isolator of claim 3 wherein each of the first, second, third, and fourth magnetoresistors comprises a serpentine structure having a plurality of elongated magnetoresistive portions coupled end-to-end, wherein the elongated portions of the first and second magnetoresistors are positioned near and in parallel to a first elongated portion of each of the turns of the input strap, wherein the elongated portions of the third and fourth magnetoresistors are positioned near and in parallel to a second elongated portion of each of the turns of the input strap, wherein the first elongated portions of the turns of the input strap carry current in a direction that is opposite to current carried by the second elongated portions of the turns of the input strap, and wherein the first elongated portions of the

turns of the input strap are parallel to the second elongated portions of the turns of the input strap.

5. (previously presented) The integrated signal isolator of claim 37 wherein each of the first, second, third, and fourth magnetoresistors comprises a serpentine structure having a plurality of elongated magnetoresistive portions coupled end-to-end, wherein the elongated portions of the first and second magnetoresistors are positioned near and in parallel to a first elongated portion of the turn of the input strap, wherein the elongated portions of the third and fourth magnetoresistors are positioned near and in parallel to a second elongated portion of the turn of the input strap, wherein the first elongated portion of the turn of the input strap carries current in a direction that is opposite to current carried by the second elongated portion of the turn of the input strap, and wherein the first elongated portion of the input strap is parallel to the second elongated portion of the input strap.

6. (previously presented) The integrated signal isolator of claim 37 wherein the first, second, third, and fourth magnetoresistors are in a first layer,

wherein the input strap is in a second layer, and wherein the first and second layers are separate layers.

7. (original) The integrated signal isolator of claim 6 further comprising a dielectric between the input strap and the first, second, third, and fourth magnetoresistors.

8. (original) The integrated signal isolator of claim 7 wherein the dielectric is a first dielectric, wherein the integrated signal isolator further comprises a second dielectric over the input strap, and wherein the first, second, third, and fourth magnetoresistors are formed over a substrate and under the first dielectric.

9. (previously presented) The integrated signal isolator of claim 37 further comprising a set-reset coil having a plurality of clockwise turns and a plurality of counterclockwise turns, wherein the set-reset coil momentarily sets and resets a direction of magnetization of the first, second, third, and fourth magnetoresistors, wherein each clockwise turn of the set-reset coil has a portion running across the first and fourth magnetoresistors, wherein each counterclockwise

turn of the set-reset coil has a portion running across the second and third magnetoresistors, and wherein the clockwise and counterclockwise turns are arranged so that current supplied to the set-reset coil flows through the portions of each of the clockwise and counterclockwise turns in the same direction.

10. (previously presented) The integrated signal isolator of claim 37 further comprising a set-reset coil having a plurality of turns disposed with respect to the first, second, third, and fourth magnetoresistors so that the set-reset coil generates a momentary magnetic field across the first, second, third, and fourth magnetoresistors in the same direction.

11. (currently amended) An integrated signal isolator having first and second ends, wherein the integrated signal isolator comprises:

first, second, third, and fourth magnetoresistors located between the first and second ends, wherein the first and second magnetoresistors are coupled in series from a first power supply terminal to a second power supply terminal, wherein the third and fourth magnetoresistors are coupled in series from the

second power supply terminal to the first power supply terminal, wherein a junction between the third and fourth magnetoresistors is coupled to a first isolator output terminal, wherein a junction between the first and ~~fourth~~ second magnetoresistors is coupled to a second isolator output terminal, and wherein the first and second power supply terminals cause a current to flow in a direction though the first, second, third, and fourth magnetoresistors; and,

an input strap having at least one turn coupled between first and second isolator input terminals, wherein the at least one turn has a first portion extending from the first end to the second end and running lengthwise alongside only the first and second magnetoresistors and a second portion extending from the second end to the first end and running lengthwise alongside only the third and fourth magnetoresistors, wherein the at least one turn is arranged so that current supplied to the input strap flows through the first portion in a first direction from the first end to the second end and through the second portion in a second direction from the second end to the first end, wherein the first and second directions are substantially opposite to one another, and wherein the first and second

directions of current flowing through the input strap are parallel to the direction of current flow through the first, second, third, and fourth magnetoresistors.

12. (original) The integrated signal isolator of claim 11 wherein the input strap includes a plurality of turns.

13. (original) The integrated signal isolator of claim 11 wherein the first, second, third, and fourth magnetoresistors are in a first layer, wherein the input strap is in a second layer, and wherein the first and second layers are separate layers.

14. (original) The integrated signal isolator of claim 11 further comprising a dielectric between the input strap and the first, second, third, and fourth magnetoresistors.

15. (original) The integrated signal isolator of claim 14 wherein the dielectric is a first dielectric, wherein the integrated signal isolator further comprises a second dielectric over the input strap, and wherein the

first, second, third, and fourth magnetoresistors are formed over a substrate and under the input strap.

16. (previously presented) The integrated signal isolator of claim 11 further comprising a set-reset coil having a plurality of clockwise turns and a plurality of counterclockwise turns, wherein the set-reset coil momentarily sets and resets a direction of magnetization of first, second, third, and fourth magnetoresistors, wherein each clockwise turn of the set-reset coil has a portion running across the first and fourth magnetoresistors, wherein each counterclockwise turn of the set-reset coil has a portion running across the second and third magnetoresistors, and wherein the clockwise and counterclockwise turns are arranged so that current supplied to the set-reset coil flows through the portions of each of the clockwise and counterclockwise turns in the same direction.

17. (previously presented) The integrated signal isolator of claim 11 further comprising a set-reset coil having a plurality of turns disposed with respect to the first, second, third, and fourth magnetoresistors so that the set-reset coil generates a

momentary magnetic field across the first, second, third, and fourth magnetoresistors in the same direction.

18. (withdrawn) A method of isolating first and second circuits comprising:

generating a first field across at least one magnetically responsive element, wherein the first field is generated in response to an isolator input signal from the first circuit;

generating a second field across at least another magnetically responsive element, wherein the second field is generated in response to the isolator input signal from the first circuit, and wherein the first and second fields are substantially opposite to one another in direction; and,

supplying an isolator output signal to the second circuit, wherein the isolator output signal is derived across the at least two magnetically responsive elements, and wherein the first and second fields are generated so that the isolator output signal is responsive to the isolator input signal that generates the first and second fields but not to an external field.

19. (withdrawn) The method of claim 18 wherein the first field is generated across the first and second magnetically responsive elements and the second field is generated across third and fourth magnetically responsive elements, wherein the first and second magnetically responsive elements are coupled to a first isolator output terminal, wherein the second and third magnetically responsive elements are coupled to a first supply terminal, wherein the third and fourth magnetically responsive elements are coupled to a second isolator output terminal, and wherein the first and fourth magnetically responsive elements are coupled to a second supply terminal.

20. (withdrawn) The method of claim 18 wherein the first field is generated across the first and third magnetically responsive resistors and the second field is generated across second and fourth magnetically responsive resistors, wherein the first and second magnetically responsive elements are coupled to a first isolator output terminal, wherein the second and third magnetically responsive elements are coupled to a first supply terminal, wherein the third and fourth magnetically responsive elements are coupled to a second

isolator output terminal, and wherein the first and fourth magnetically responsive elements are coupled to a second supply terminal.

21. (withdrawn) The method of claim 18 wherein the first field is generated across the first and fourth magnetically responsive resistors and the second field is generated across second and third magnetically responsive resistors, wherein the first and second magnetically responsive elements are coupled to a first isolator output terminal, wherein the second and third magnetically responsive elements are coupled to a first supply terminal, wherein the third and fourth magnetically responsive elements are coupled to a second isolator output terminal, and wherein the first and fourth magnetically responsive elements are coupled to a second supply terminal.

22. (withdrawn) The method of claim 18 further comprising setting the magnetic moments of the at least two magnetically responsive elements in the same direction.

23. (withdrawn) The method of claim 22 wherein the moment direction is substantially perpendicular to the first and second fields.

24. (withdrawn) The method of claim 23 wherein the setting of the magnetic moments is momentary.

25. (withdrawn) The method of claim 24 wherein the setting of the magnetic moments comprises setting the magnetic moments prior to generating the first and second fields.

26. (withdrawn) A method of making an integrated signal isolator having first and second ends comprising:

forming first, second, third, and fourth magnetoresistors in a first layer of an integrated structure so that the first and second magnetoresistors are substantially aligned along a first axis, so that the third and fourth magnetoresistors are substantially aligned along a second axis, and so that the first axis is offset from and parallel to the second axis;

coupling the first and second magnetoresistors to a first isolator output terminal;

coupling the second and third magnetoresistors to a first supply terminal;

coupling the third and fourth magnetoresistors to a second isolator output terminal;

coupling the first and fourth magnetoresistors to a second supply terminal;

forming an input strap in a second layer of the integrated structure so that the input strap, when receiving an input, generates a field across two of the first, second, third, and fourth magnetoresistors and an opposing field across the other two of the first, second, third, and fourth magnetoresistors; and,

coupling the input strap between first and second isolator input terminals.

27. (withdrawn) The method of claim 26 wherein the each of the first, second, third, and fourth magnetoresistors comprises a corresponding serpentine structure.

28. (withdrawn) The method of claim 26 further comprising forming a dielectric between the input strap and the first, second, third, and fourth magnetoresistors.

29. (withdrawn) The method of claim 26 further comprising forming a set-reset coil in a third layer of the integrated structure.

30. (withdrawn) The method of claim 29 wherein the second layer is between the first and third layers.

31. (currently amended) The integrated signal isolator of claim ~~1~~ 37 wherein the input strap is disposed with respect to the first, second, third, and fourth magnetoresistors so that, when input current flows between the first and second isolator input terminals, a resistance of the first magnetoresistor tracks a resistance of the third magnetoresistor, and a resistance of the second magnetoresistor tracks a resistance of the fourth magnetoresistor.

32. (currently amended) The integrated signal isolator of claim ~~1~~ 37 wherein the input strap has a first portion running along a length of the two of the magnetoresistors and a second portion running along a length of the other two of the magnetoresistors.

33. (previously presented) The integrated signal isolator of claim 32 wherein the first portion runs along the length of the first and second magnetoresistors and the second portion runs along the length of the third and fourth magnetoresistors.

34. (currently amended) The integrated signal isolator of claim ~~1~~ 37 further comprising a set/reset strap positioned to generate a momentary set/reset magnetic field over the magnetoresistors.

35. (previously presented) The integrated signal isolator of claim 34 wherein the set/reset strap perpendicularly crosses a length of the magnetoresistors in the same direction so as to carry current across the magnetoresistors in the same direction.

36. (previously presented) A semiconductor signal isolator having first and second ends, wherein the semiconductor signal isolator comprises:

first and second isolator input terminals;

first and second isolator output terminals;

first and second power supply terminals;

a semiconductor substrate;

first, second, third, and fourth magnetoresistors formed in at least one layer over the semiconductor substrate, wherein the first and second magnetoresistors are coupled in series from the first power supply terminal to the second power supply terminal, wherein the third and fourth magnetoresistors are coupled in series from the second power supply terminal to the first power supply terminal, wherein the first isolator output terminal is coupled to a junction between the first and second magnetoresistors, wherein the second isolator output terminal is coupled to a junction between the third and fourth magnetoresistors, and wherein the first and second power supply terminals cause a current to flow in a direction though the first, second, third, and fourth magnetoresistors;

an input strap formed in at least one layer over the semiconductor substrate, wherein the input strap has at least one turn coupled between the first and second isolator input terminals, wherein the input strap is disposed with respect to the first, second, third, and fourth magnetoresistors so that a magnetic field is generated over the first and second magnetoresistors in one direction, and so that a magnetic field is generated

over the third and fourth magnetoresistors in an opposite direction, and wherein current flows through the input strap in a direction parallel to the direction of current flow through the first, second, third, and fourth magnetoresistors; and,

a dielectric between the input strap and the first, second, third, and fourth magnetoresistors.

37. (previously presented) An integrated signal isolator having first and second ends, wherein the integrated signal isolator comprises:

first and second isolator input terminals to receive a signal to be isolated;

first and second isolator output terminals to provide an isolated output signal;

first and second power supply terminals;

first, second, third, and fourth magnetoresistors, wherein the first and second magnetoresistors are coupled in series from the first power supply terminal to the second power supply terminal, wherein the third and fourth magnetoresistors are coupled in series from the second power supply terminal to the first power supply terminal, wherein the first isolator output terminal is coupled to a junction

between the first and second magnetoresistors, wherein the second isolator output terminal is coupled to a junction between the third and fourth magnetoresistors, and wherein the first and second power supply terminals cause a current to flow in a direction though the first, second, third, and fourth magnetoresistors; and,

an input strap having at least one turn coupled between the first and second isolator input terminals, wherein the input strap is disposed with respect to the first, second, third, and fourth magnetoresistors so that a magnetic field is generated over the first and second magnetoresistors in one direction, and so that a magnetic field is generated over the third and fourth magnetoresistors in an opposite direction, and wherein the current through the input strap flows in a direction parallel to the direction of current flow through the first, second, third, and fourth magnetoresistors.